IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Jean-Michel Daga et al. PATENT APPLICATION
Serial No.: 10/810,033 Group Art Unit: 2816
Filed: March 26, 2004 Examiner: A.Q. Tra
Confirmation No.: 8427 Atty. Docket No.: ATM-276
For: HIGH EFFICIENCY, LOW COST, CHARGE PUMP CIRCUIT

DECLARATION OF PRIOR INVENTION IN WTO COUNTRY TO OVERCOME CITED PUBLICATION (37 C.F.R. § 1.131)

1. This declaration is to establish conception of the invention of U.S. Patent Application No. 10/810,033 prior to September 24, 2003, the effective filing date of U.S. Patent Application Publication No. 2004/0104761, a reference cited by the examiner in an Office action regarding U.S. Patent Application No. 10/810,033.

2. Jean-Michel Daga and Emmanuel Racape are the named inventors of U.S. Patent Application No. 10/810,033, "High Efficiency, Low Cost, Charge Pump Circuit," filed March 26, 2004 in the U.S. Patent and Trademark Office.

3. Jean-Michel Daga and Emmanuel Racape disclosed the invention in an invention disclosure form submitted to Atmel Corporation's legal department on August 14, 2003. A copy of this invention disclosure form is attached as Exhibit A.

4. All inventive acts described in the French and U.S. patent applications took place in France, a WTO country. Patent drafting activity by Atmel Corporation's legal counsel took place in the United States.

5. As a person signing below, I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true. These statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States code, and that such willful false statements may jeopardize the validity of U.S. Patent Application No. 10/810,033 or any patent issued thereon.

Signature _____ Date 12/16/2005
Jean-Michel Daga

Signature _____ Date 12/16/2005
Emmanuel Pacape

Attachments: Exhibit A

EXHIBIT A

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ATMEL LEGAL DEPT.

ATMEL CORPORATION: INVENTION DISCLOSURE
ATTORNEY CLIENT COMMUNICATION
ATMEL PROPRIETARY INFORMATION

I. TITLE OF INVENTION (short and descriptive):

High Efficiency, Low Cost Charge pump circuit

II. INVENTOR(S) INFORMATION:[1]

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III. BRIEF DESCRIPTION OF THE INVENTION: (One or two concise paragraphs.)

Charge pump circuit with optimal gain per stage, and fully compatible with a standard, advanced CMOS process.

C. First Disclosure To Others At Atmel: WHERE, WHEN AND TO WHOM (Specify and supply copies of all documents describing first disclosure.):

D. Give Dates and Details Regarding Samples, Information or Publications Relating To the Invention Which Have Been or Will Be Given To Persons Outside of Atmel (Specify and supply copies of all documents describing samples and publications.)[2]

E. Has any Product Resulting From the Practice Referred To In Question No. IV(B), Been Offered For Sale or Sold? If So, WHEN, WHERE AND TO WHOM? (Specify and supply copies of all documents relating to such offer for sale or sale.):

NO

F. If The Invention Is Embodied In An Apparatus, Article, Circuit, Composition of Matter, Compound, Software, Etc. Has It Been Offered For Sale or Sold? If So, WHEN, WHERE AND TO WHOM? (Specify and supply copies of documents describing such offer for sale or sale.):

G. If The Invention Has Not Been Practiced (Experimental Or On A Larger Scale) When Is Use Of the Invention Expected To Begin?

First Experimental Test Chip END 2003. Product in 2004.

[2] All such disclosures outside of Atmel MUST be pursuant to Atmel's Non-Disclosure Agreement, a copy of which you can obtain from the Legal Department.

03-34

High efficiency, low cost charge pump circuit

Previous art

Charge pump circuits are used to provide a voltage that is higher than the voltage of the power supply, or a voltage of reverse polarity. These circuits are commonly used in Flash and EEPROM memories, but are gaining more and more acceptance in analog circuits in order to increase the dynamic range and simplify the design. The most popular approach is the Dickson charge pump, which switched capacitor based circuitry is given in Figure 1. Each stage is made of a capacitor and a NMOS type transistor acting as a diode. These transitors have their bulk connected to the ground, their drain and gate connected together to the stage capacitor, and their source connected to the capacitor of the next stage. Two inverted phase clocks are used, and the maximum gain per stage is VDD-VT, where VT is the threshold voltage of the NMOS device. As the supply voltage decreases with advanced technologies the pumping efficiency of such charge pump is decreased. Moreover, the body effect that increases the threshold voltage of the NMOS devices when the drop between their source and bulk increases, limits the number of stages that can be cascaded. Another important drawback of such structure is that thick oxide, high voltage dedicated transistors are necessary to sustain large drop between gate and bulk in a reliable way. This makes it impossible to design such circuit using thin oxide, low voltage standard devices which can sustain a maximum drop of VDD.

Many improvements to the basic Dickson structure have been added to overcome the gain degradation due to the threshold voltage. Among the large number of proposed solutions, the four phase structure of [1] is a very efficient approach to prevent gain degradation due to threshold voltage. 9V output is obtained using a ten stage pump, starting from 1V power supply. Anyway, high voltage devices are still necessary, making this approach not usable on standard CMOS process. A solution has been proposed to use low voltage transistors, using two phase clocking scheme [2]. However, NMOS devices on triple well technology are used, keeping the need of additional masking and process steps compared to standard CMOS process.

The charge pump circuitry of the present invention alleviates all the limitations of the previous solutions: there is no limitation to the gain per stage due to threshold voltage and body effect on NMOS devices, low voltage devices can be used without any restriction such as the need of a deep nwell. The basic idea of the present invention is to use PMOS devices to realize the switches, while maintaining a maximum voltage drop on the transistors lower than VDD.

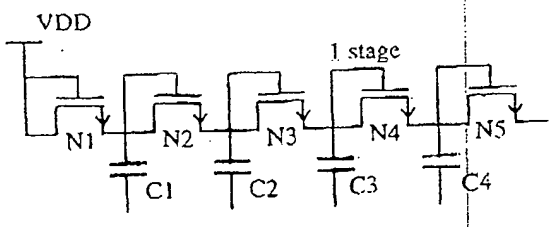

Figure 1. Dickson charge pump

Word + Email

Description of the proposed invention

First (and preferred) implementation

The Figure 2 describes the basic stage of the proposed charge pump invention. This is a symmetrical structure composed of 6 low voltage PMOS devices (P1, P2, P3, P4, P5, P6), two boosting capacitors (C_{pump1} and C_{pump2}) and two auxiliary capacitors (C_{aux1} and C_{aux2}). Each device and its symmetrical counterpart are identically sized. A N stage charge pump can be obtained by cascading N basic stages, as shown in Figure 3. The four phases necessary for the correct operation of the structure are described on Figure 4. The clock signal variation is between 0 and VDD. Assuming Vin at the input, basic operation of the pump stage components is as follows: Cpump1 (Cpump2) is a large coupling capacitor used for the basic charge pumping operation. P2 (P5) device is used to transfer the charges from the pumping node pump1 (pump2) to the output, and prevent reversal current feedback from the output to the pumping node. P1 (P4) is used to connect the pumping node pump1 (pump2) to the input Vin when Cpump1 (Cpump2) is not pumped, that is to say when Φ1 (Φ2) is low. P3 (P6) is used to switch the gate of P1 (P4) to the boosted pump node potential in order to prevent reversal current feedback to the input when Cpump1 (Cpump2) is boosted. Auxiliary small capacitor Caux1 (Caux2) is used to generate an under-shoot on the gate of P1 (P4) and have this device ON when the charges are transferred from the input to the pumping node pump1 (pump2).

Detailed description of the first implementation in steady state

In steady state, pumping node netpump1 (netpump2) varies from Vin to Vin + Cr1.VDD where Cr1=1/(1+Cpar1/Cpump1). Cpar1 is the total parasitic capacitance at node netpump1, due to P1, P2, P3 and P5 devices. Assuming that Cpump1>>Cpar1, Cr1 is very closed to 1, resulting in an approximated variation of the pumping node between Vin and Vin+VDD. The auxiliary node netaux1 (netaux2) switches to Vin+2VDD during the pumping of node netpump1 (netpump2) thanks to the P3 (P6) device ON. At the end of the pumping operation, Φ1 (Φ2) goes low, netpump1 (netpump2) and netaux1 (netaux2) decrease to Vin. Then, Φ1aux (Φ2aux) switches low to drive the auxiliary node netaux1 (netaux2) below Vin and turn P1 device ON. The potential at node netaux1 (netaux2) during the under-shoot is equal to Vlow, where **Vlow = Vin – Cr2.VDD**, where Cr2=1/(1+Cpar2/Caux1). Cpar2 is the total parasitic capacitance at node netaux1 due to P1 and P3 devices. The condition to be respected to achieve a correct functionality is Cr2.VDD>Vt, where Vt is the threshold voltage of the P device.

Detailed description of the pump stage operation during one period can be done starting from the following initial conditions: Φ1 and Φ1aux are low, Φ2 and Φ2aux are high. Nodes netpump2 and netaux2 are to Vin+VDD (assuming Cr1=1 to simplify), netpump1 is to Vin and netaux1 to Vlow. Now Φ1aux switches to VDD, netaux1 rises from Vlow to Vin thanks to the Caux1 coupling capacitor. Then the clock Φ1 switches to VDD, netpump1 node rises to Vin+VDD, as well as the node netaux1 which is connected to netpump1 through P3 device. At the next phase Φ2 goes low, switching netpump2 node to Vin, as well as netaux2 through P6 device. Because netpump2 is now to Vin, P2 device turns ON and charge transfer from the pumping node netpump1 to the output occurs. Because P1 and P5 have their gate connected to Vin+VDD, they are OFF and there is no reversal charge transfer. During the last phase, Φ2aux goes low in order to switch netaux2 to Vlow and turn P4 ON to transfer the charges from the input to netpump2 node that will be the next pumped node. During the first half period charges are transferred from the netpump1 node to the output, and from the input to

netpump2. When charge transfer is completed, the symmetrical second half period can start by switching Φ2aux high in order to rise netaux2 from Vlow to Vin. Then Φ2 pulses high to boost netpump2 and aux2 to Vin+VDD, followed by Φ1 pulsing low to turn P5 ON to start charge transfer from netpump2 to the output. Last phase consists in switching Φ1aux low to turn P1 ON. During this second half period charges are now flowing from the input to the next pumped node netpump1, and from the pumped node netpump2 to the output.
The charge transfer is not limited. The voltage gain of the stage is Cr1.VDD, and can be made very closed to VDD by correct sizing of the devices and capacitors, in order to make parasitic capacitance negligible.
A very important characteristic of the structure is that the voltage drop between the four nodes of each device does not exceed VDD during the pump operation. Moreover the bulk of the P devices is always at the higher potential.
N stage charge pump can be obtained by cascading basic stages as shown on Figure 4. The gain per stage is only limited by parasitic capacitance and can be made very closed to VDD. Assuming N stage charge pump with Vin at the input, maximum output value that can be obtained if no current is pulled at the output is Vin+N.Cr1.VDD.
10.6V output voltage has been obtained on a 10 stages charge pump using 0.18µm devices, with a power supply of 1V. This represents 96% of VDD average gain per stage on a 10 stage structure.

Second implementation

Another implementation of the charge pump based on the same approach is possible. Figure 5 shows the basic stage of the second implementation. The only difference with the first basic structure of Figure 2 is that P3 and P6 devices can be controlled independently using ctrlin1 and ctrlin2 input signals. The charge pump realization using this basic stage is shown in Figure 6. The first stage is identical to the first implementation because ctrlin1 and ctrlin2 are connected to Vin. On the next stages, ctrlin1 (ctrlin2) is connected to the ctrlout1 (ctrlout2) output of the previous stage. Using this structure, during the pumping operation on the node netpump1, the voltage difference between the drain and the gate of the P3 device is 2VDD, instead of VDD using the first structure. When the node netpump1 is not pumped, the conditions on the P3 device are the same as in the first implementation. The same occurs in a symmetrical way with P6 device when the node netpump2 is boosted. This structure is perfectly functional, and has the same level of performance as the first implementation. Anyway, P3 and P6 devices suffer a maximum of 2VDD between their drain and gate during pumping, making their implementation using low voltage, thin oxide devices impossible. So specific devices, with thicker oxide are needed for P3 and P6. This is a main drawback compared to the first implementation.

Advantages of the proposed invention

Both structures

Optimal gain per stage: no degradation due to the threshold voltage, gain per stage limited by parasitics only, perfectly suitable for low voltage operation.

Preferred implementation (first structure)

Use of low voltage, thin oxide device (maximum voltage drop between nodes of VDD): Fully compatible with a CMOS standard process.

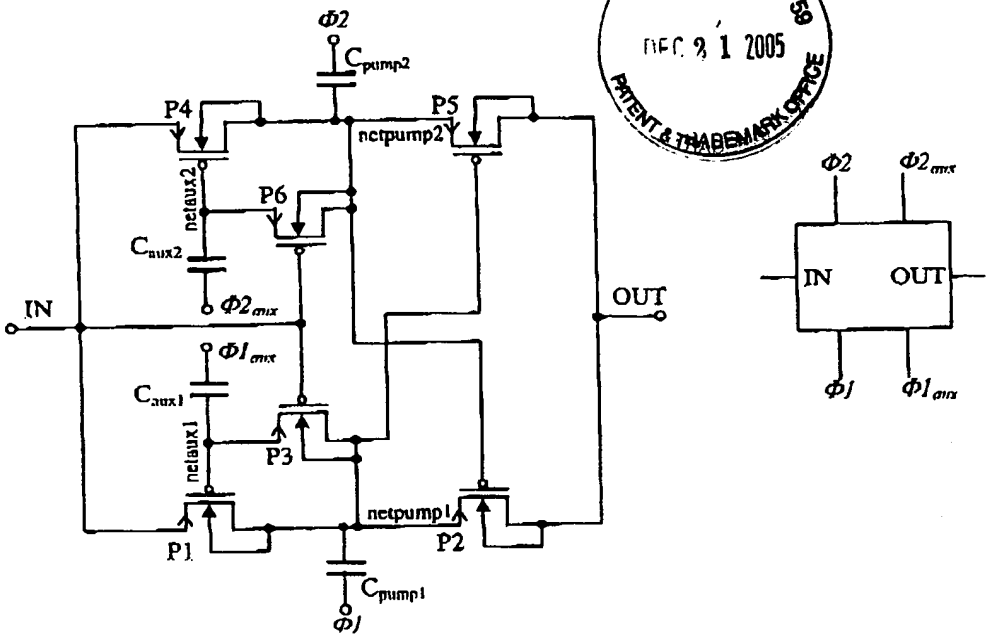

Figure 2. Basic pump stage of the first implementation

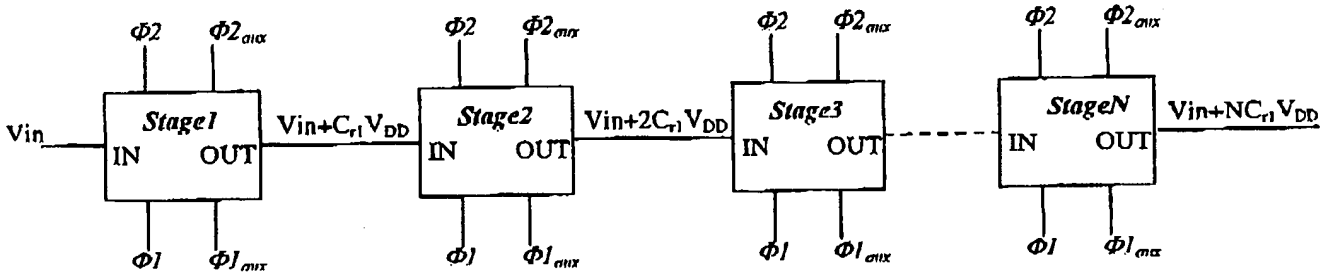

Figure 3. First implementation of the charge pump using basic stage of Figure 2

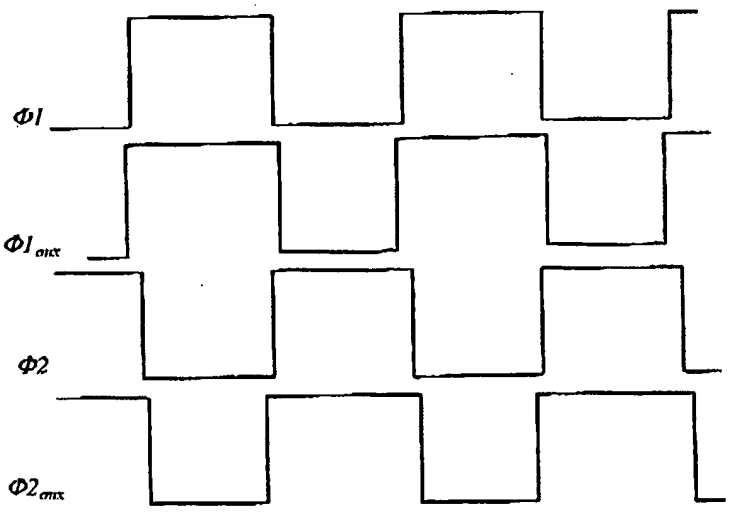

Figure 4. Clocking scheme

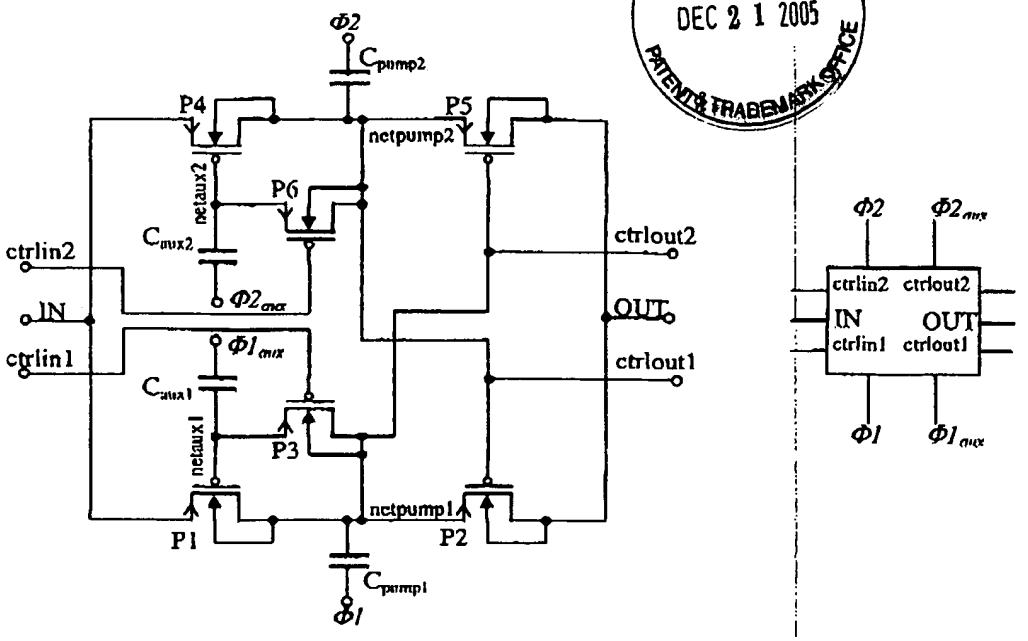

Figure 5. Basic pump stage of the second implementation

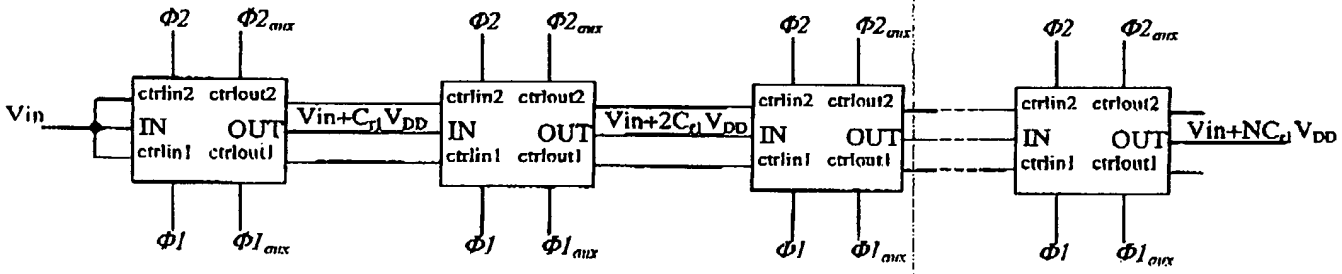

Figure 6. Second implementation of the charge pump using basic stage of Figure 5

References

⇒ [1] Hongshin Lin and Nai-Hsien Chen, "New Four-Phase Generation Circuits For Low-Voltage Charge Pumps", Proc. ISCAS'2001

[1] F. Pulvirenti, U.S. Patent 5874850, Feb. 23, 1999